REMARKS

Claims 1-33 are pending. Claims 11-12, 16, 23 and 26-27 are considered to have allowable subject matter.

Claim 1 is proposed to be amended to recite a "DC offset implemented in at least one of at the input stage, in the input stage, or in the feedback circuit to set the DC bias voltage at the output terminal". Support for this amendment is found in [0117]-[0121], referring to Figs. 10a and 10b of the U.S. publication 2007/0076804. Applicant also submits that Fig. 10a by itself in an unambiguous manner discloses the various recited injection points for the DC offset by virtue of the depicted (virtual) DC offset sources 1001, 1002 and 1003.

A new claim 34 is proposed to be added that is dependent from amended claim 1. This claim sets forth that the DC offset can be accomplished at a group of the locations of those set forth in Fig. 1.

With respect to the proposed amendment to claim 1, the recited structure accomplishes that the DC bias voltage at the output terminal is set to an appropriate DC level. Typically this would be about midway between the positive (Vdd) and negative (GND) supply rail, to allow the AC voltage at the output terminal to swing maximally without output signal limiting or distortion.

Claim 2 is proposed to be amended to clarify the circuit connection. Support for this is derived from [0118] of the patent publication, in particular the last sentence thereof.

Claims 13-17 claim various structures and functions for implementing the DC offsets. Claim 15 is proposed to be amended to recite that the claimed ohmic impedance can be provided by any one of a resistor, a diode and an active device. The basis for this amendment can be derived from [0119]-[0120], referring to Figs. 10b and 10c, which show the claimed types of ohmic impedances. A few minor amendments are proposed to be made to claim 17 to make the terminology consistent with claim 1.

The allowability of claims 11-12, 16, 23 and 26-27 is noted. These claims now include the subject matter of claim 1 as proposed to be amended. Applicant reserves the right to reinstate these claims written in proper form without the proposed amendment to claim 1.

Claims 1-2, 8-10, 13-15, 17-18, 20-22, 25, 28-29 and 31-33 are rejected as being unpatentable over Fig. 2 of the AAPA (Eschauzier, et al.), U.S. 6,160,450.

Claims 3-4 are rejected as unpatentable over the AAPA in view of Tsinker, U.S. 6,150,875.

Claims 5-7 are rejected as unpatentable over the AAPA in view of Bhandari, et al., U.S. 6,424,480.

Claims 19 and 20 are rejected as unpatentable over the combination of the AAPA in view of French, U.S. 5,337,011.

Claim 1 is the main independent claim from which the other claims depend. This claim is proposed to be amended as discussed above relative to the DC offset.

Applicant first notes that the circuit of Fig. 2 of the AAPA, on which the rejection of main claim 1 is based, is stated in the AAPA patent (column 2, lines 10-15) not to be able to function as desired. That is, it is basically inoperative for its intended function. The Examiner's obviousness rejections from page 3 of the Office Action and onward are generally based on finding the majority of the claimed features in the AAPA Fig. 2 circuit and then combining these features with allegedly well-known features in the art. Applicant respectfully submits that this line of argumentation is fundamentally flawed because of the admitted inoperability problem of the AAPA Fig. 2 circuit. The skilled person in the art will certainly not be inclined or motivated to take the AAPA Fig. 2 circuit as a starting point for developing the claimed invention.

In the proposed amendment to claim 1, the recited structure accomplishes that the DC bias voltage at the output terminal is set to an appropriate DC level. This has the effect that the distortion level of the output signal of the microphone preamplifier is minimized and the dynamic range of the output signal is maximized. Setting the appropriate DC level on the output terminal is particularly important for mass produced low-voltage microphone preamplifiers because these are normally forced to operate from a very low DC supply voltage (i.e., the difference between the positive (Vdd) and negative (GND) supply).

The magnitude of the optimal DC offset for any specific microphone amplifier design will depend on the actual injection point or points and the DC gain of the preamplifier. Typically, the best effect would be accomplished by selecting the DC offset in a manner where the DC bias voltage at the output terminal would be set about midway between the positive (Vdd) and negative (GND) supply rail, to, as previously explained, allow the AC voltage at the output terminal to swing with minimum distortion and minimum output signal limiting.

The proposed amendment to claim 1 relative to the DC offset provides a novel and advantageous preamplifier. The circuit of the invention is much simpler than that of Fig. 3 of the AAPA and provides a relatively distortion-free circuit. Also, the invention avoids the loading of the electret microphone provided by the LPF (R1-R2-C1) of Fig. 3 of the AAPA. This loading is highly undesirable for miniature electret microphones that act as extremely high impedance signal generators, and may lead to incorrect frequency response and high noise levels.

Accordingly, claim 1 defines a novel and advantageous circuit. The claim is patentable and should be allowed.

Applicant also respectfully submits that the Examiner's obviousness rejection based on the AAPA Fig. 2 circuit against each of the dependent claims 13-17 is entirely erroneous. None of the claimed features (related to implementing the DC offset) of these claims are disclosed in connection with the AAPA Fig. 2 circuit.

With respect to new claim 34, the Examiner should note that distributing the DC offsets between the input stage and the feedback circuit can lead to a more optimal way of providing a desired total DC offset without undue substrate die area consumption or increased noise as described in the last sentence of [0118].

For example, if the entire DC offset is implemented solely in the input stage this may create large imbalances in the input stage due to much differently sized input transistors or differently biased input transistors. This can lead to excessive die area consumption, increased noise and deteriorating power supply rejection.

With respect to claim 15, the Examiner should note that claimed structure for implementing the DC offset at the input stage is advantageous compared to the AAPA Fig. 4 circuit. The latter circuit creates a DC offset in the input stage by resistor R_{offset} leading to some of the above-mentioned imbalance problems. In addition, the AAPA Fig. 4 circuit lacks the claimed low pass filter in the feedback path as previously discussed.

It is demonstrated above that the proposed amendments to main claim 1 clearly define a circuit that is patentable. Therefore, claim 1 and its dependent claims 1-2, 8-10, 13-15, 17-18, 20-22, 25, 28-29 and 31-33 that are rejected over only the AAPA are patentable and should be allowed.

The claims that are rejected over the AAPA in view of a secondary reference also are patentable. The addition of the secondary reference does not cure the basic defect of the AAPA with respect to claim 1, from which all of these claims depend. Therefore, these claims also are allowable.

The amendment should be entered since it places the application in condition for allowance. It does not raise any new issues that require further search.

If the amendment is not entered as placing the application in condition for allowance, then its entry is requested for purposes of appeal.

Prompt and favorable action is requested.

Dated: March 19, 2009

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